AIR BRIDGE GATE FET FOR GaAs MONOLITHIC CIRCUITS

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ABSTRACT

The paper describes a novel technology for producing micron and submicron gate FET devices, with improved gain and noise performances.

The technique is particularly attractive for the production of very low noise devices and is very useful in monolithic circuit fabrication.

In the production of high-power devices the technique has the advantage of not requiring complicated interdigitated structures. A noise figure improvement of 0.4 dB at 10 GHz was achieved using this technology. As an example of the developed technique, a two-stage monolithic preamplifier (2.8 dB N.F., 15 dB gain between 11.7 and 12.5 GHz) is described.

INTRODUCTION

It is well known that the noise and gain performances of FET devices can be enhanced by reducing the device gate length.

The good performances, for a given gate length, are strictly related to the reduction of the distributed gate resistance R_g and of the source resistance R_s. FET's with gate lengths lower than .5 μm cannot be practically used in the monolithic circuit fabrication since their yield is too low. For this reason it is important to set up a simple high-yield process to realize monolithic circuits where the active devices are .5 μm gate FET's with very low gate and source resistances. The source resistances of discrete devices are frequently reduced using recessed gate structures. However, because of the complications inherent in the process, this choice is rather unpractical. An allowable way of reducing the device source resistance is the use of n^+ contacts under the source and drain metalizations. This can be easily obtained through selective ion implantation. On the other hand, some technological limits exist in reducing the gate metalization resistance. The increase in the gate metalization thickness is limited by the difficulty of the submicron line definition. Strong decrease in the single gate arm width requires complicated interdigitated structures (especially for power FET structures).

THE NOVEL TECHNOLOGY

This work deals with a new FET structure*) allowing a drastic reduction of the distributed gate resistance to be obtained. The paper will describe the new structure and report the relevant technological process. The advantages of the structure as for noise and gain performances will be discussed. As an example of application, a monolithic two-stage amplifier will be described, which was developed for use in a high-yield fully monolithic DBS front-end receiver recently constructed for mass production[1].

In order to well understand the new device structure, figs. 1a and 1b show the conventional FET structure and the air bridge gate FET, respectively.

In the proposed new structure, the gate electrode consists of an air bridge connection over the source electrode. The air bridge structure connects the gate pad at the one end and the gate electrode along its whole width at the other. In fig. 2 a cross section of the structure is shown.

In this way a much lower metalization resistance can be attained in comparison with the conventional gate structure in fig. 1a. The technology to achieve this structure is quite similar to the well known air bridge technology and is well-suited to the monolithic fabrication.

In fig. 3 an example of the technological process is shown.

Starting from the source and drain pads (fig. 3a) the gate length and the gate pads are defined by standard conventional photolithography. Afterwards, a gate metalization is evaporated over the whole wafer (fig. 3b). Electrolytic gold is successively grown on the gate metalization ($t \sim 4 \div 5$ μm) and a second photoresist layer is deposited and masked to define the air bridge connection (fig. 3c). Finally, the electrolytic gold layer and the gate metalization are etched-off through the photoresist mask and the two photoresist layers are removed to get the wanted structure in fig. 3d.

The air gap is about 4 μm and involves a negligible parasitic capacitance.

Fig. 4 shows a scanning electron micrograph of the air bridge gate structure.

Obviously, instead of a continuous bridge along the gate, a structure with parallel-bridge strips

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can be realized, which can drastically reduce the distributed gate resistance too, but it introduces lower parasitic capacitances vs the other FET electrodes. To reduce the parasitic inductance vs ground the source contact is grounded through via-holes.

THE INFLUENCE OF THE AIR BRIDGE STRUCTURE ON THE GAIN AND NOISE PERFORMANCES OF THE DEVICES

Now suppose we construct, with the same process, two FET's, one very near the other, on the same doped GaAs substrate. The first FET (FET 1) has the topology in fig. 1a, while the second (FET 2) has the topology in fig. 1b. We impose that the following parameters are equal in both cases:

Z = total gate width, L = gate length,
L_{GS} = gate-source spacing,
L_{GD} = gate-drain spacing

In figs. 5a and 5b the equivalent circuit is reported for FET 1 and FET 2, respectively. Most of the circuit parameters in fig. 5b can be assumed to be nearly equal to those in fig. 5a since they are essentially determined by the material and the processing: $C_I \simeq C'_I$, $R_I \simeq R'_I$, $R_S \simeq R'_S$, $R_o \simeq R'_o$, $g_m \simeq g'_m$. Obviously, $R'_g \ll R_g$ and $C'_F = C_F + \Delta C_F$ ($\Delta C_F > 0$), $C'_o = C_o + \Delta C_o$.

For a source line width of 20 μm, the parasitic capacitance C'_{gs} between the gate and the source of FET 2 can be assumed $C'_g \simeq 4 \cdot 10^{-2}$ pF per millimeter of gate width.

The increase, ΔC_F, in the feedback capacitance is mainly due to the field lines between the bridge and the drain on the air side only, since, on the GaAs side, the drain is shielded by the source contact.

Such an increase, ΔC_F, is about $1.4 \cdot 10^{-2}$ pF per millimeter of gate with for distance between gate and drain of the order of one micron.

C'_o can be easily evaluated as a proximity capacitance [2], between the source and drain metals, and is mainly due to the field lines in the GaAs side.

On the basis of the above circuit considerations, it can be easily shown that the strong reduction of R_g results into a gain advantage of FET 2 over FET 1, but simultaneously it produces a shift toward the higher frequencies of the low-frequency zone of the device potential stability (K-1). The simultaneous increase of the feedback capacitance contributes to such an effect, but it limits the gain advantage.

This limit can be overcome by considering, instead of a full bridge, the comb bridge structure in fig. 6, which permits a drastic reduction of the distributed gate resistance R_g too, but it introduces lower parasitic capacitances toward the other electrodes.

The effect on device MAG of the different structures (figs. 1a, 1b and 6) is shown in fig. 7. The following parameters were chosen:
doping density $N = 2.5 \cdot 10^{17}/cm^3$, Z = 300 μm, L = .5 μm, gate metal: Au, $L_{GD} = L_{GS} = 1$ μm, gate recess: 0.4 μm x 1 μm.

For the device in fig. 1a, the gate height was: h = 0.4 μm, and for the device in fig. 7, the bridge was substituted by 17 strips, 5 μm wide.

Similar results were obtained for a .25 W recessed-gate device with $N = 1.2 \cdot 10^{17}$, Z = 600 μm, L = 0.8 μm.

In table 1 the calculated[3] minimum noise figures NF_{MIN} for different FET's are reported. As can be seen by comparing FET 3 in the table with FET's 4 and 5, in terms of reduction of the minimum noise figure, the air bridge approach is more effective than the n^+ contact approach. A minimum noise figure of 1.4 dB at 10 GHz is expected for a .5 μm gate length device having both air-bridge gate and n^+ contacts.

Fig. 8 gives the equivalent circuit of the monolithic amplifier. The matching circuit basically makes use of inductive elements with a stabilizing resistor inserted into the interstage network.

The amplifier noise performances are shown in fig. 9. The following performances were measured: N_F = 2.8 dB, G = 15 dB between 11.7 and 12.5 GHz.

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(1) E.M. Bastida, E. Cavalieri D'Oro, G.P. Donzelli, N. Fanelli, G. Fazzini, G. Simonetti: A Monolithic 800 MHz Bandwidth DBS Front-End Receiver for Mass Production, Proc. of the 14th European Microwave Conference (Liège, Belgium), pp. 755-760, 1984.

(2) R.A. Pucel et al.: Advances in Electronics and Electron Physics, 38, pp. 195-265, 1975.

(3) H. Fukui: Optimized Noise Figure of Microwave GaAs MESFET's. IEEE Transactions on Electron Devices, ED-26, pp. 1032-1037, 1979.

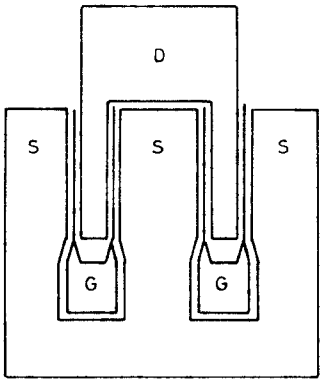

Fig. 1a - Conventional FET structure

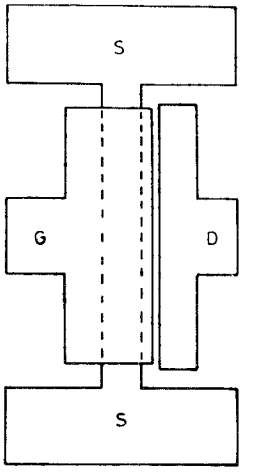

Fig. 1b - Air bridge gate FET

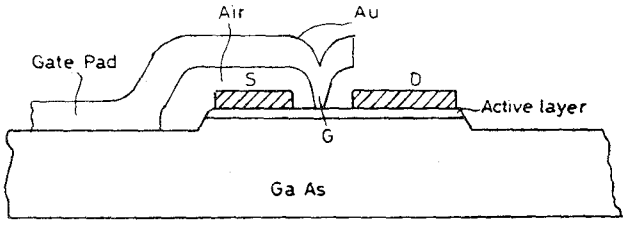

Fig. 2 - Cross section of air bridge gate FET

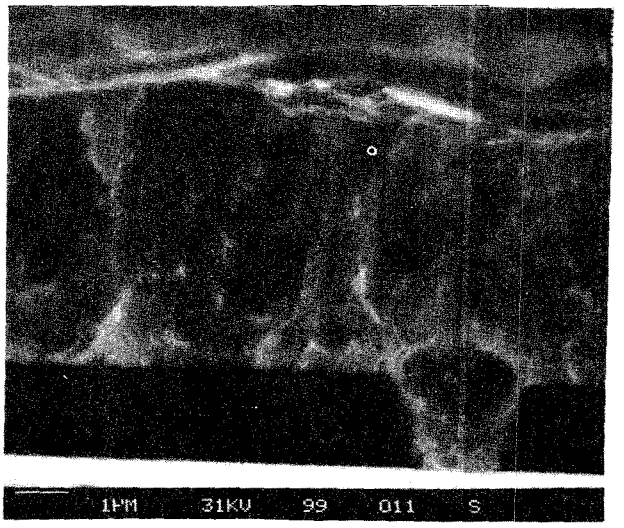

Fig. 4 - Scanning electron micrograph of air bridge gate

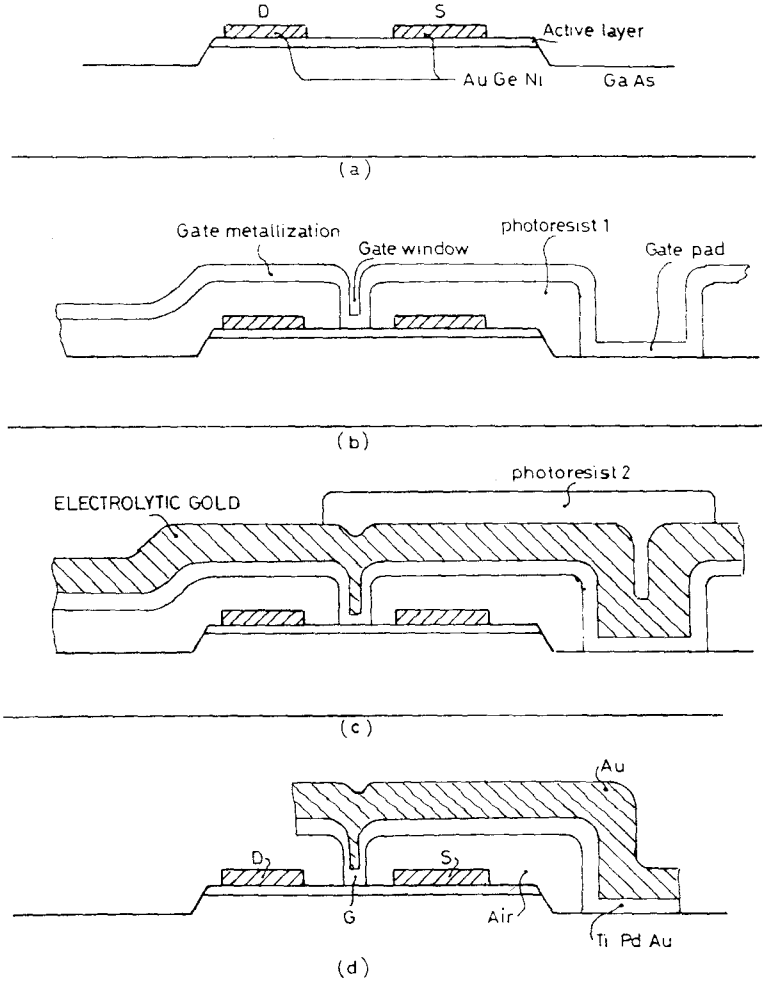

Fig. 3 - Air bridge gate technology

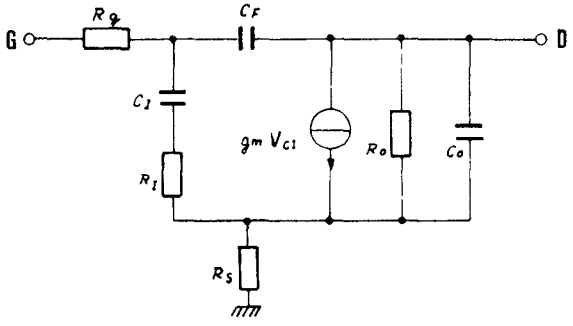

Fig. 5a - Equivalent circuit of conventional FET

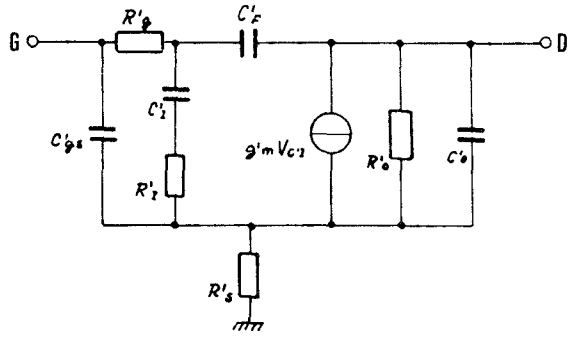

Fig. 5b - Equivalent circuit of air bridge gate

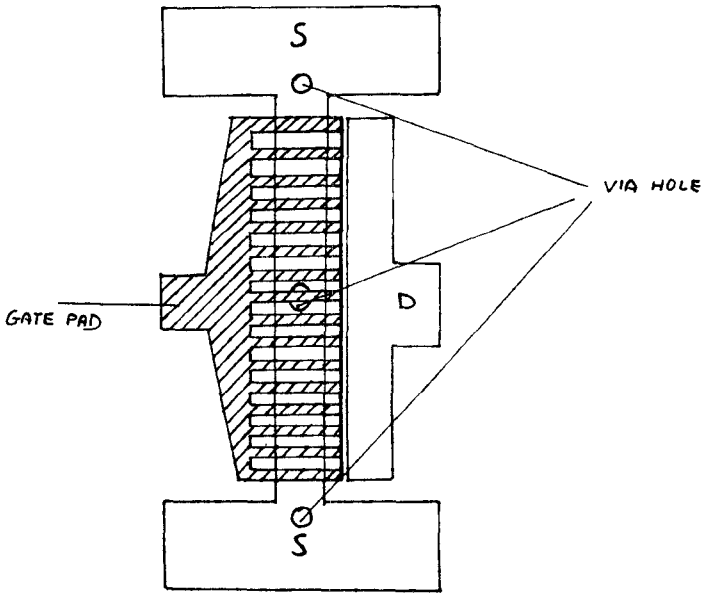

Fig. 6 - Comb-bridge gate FET

Table 1

	TOPOLOGY	n+CONTACTS	Z (mm)	z (mm)	N(cm^{-3})	L(μm)	$L_{GS}=L_{GD}$(μm)	h(μm)	a(μm)	NF_{MIN}(dB) f = 10 GHz
FET 1	fig. 1a	no	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.2	0.2	2.35
FET 2	fig. 1a	no	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.4	0.2	2.0
FET 3	fig. 1b	no	0.3	--	$2.5\ 10^{17}$	0.5	1	--	0.2	1.7
FET 4	fig. 1a	yes	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.2	0.2	2.15
FET 5	fig. 1a	yes	0.3	0.075	$2.5\ 10^{17}$	0.5	1	0.4	0.2	1.8
FET 6	fig. 1b	yes	0.3	--	$2.5\ 10^{17}$	0.5	1	--	0.2	1.4

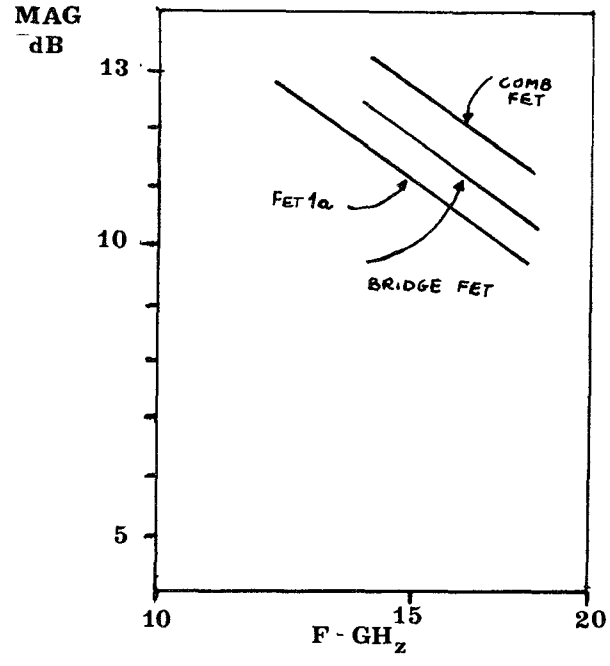

Fig. 7 - MAG of the three different FET's

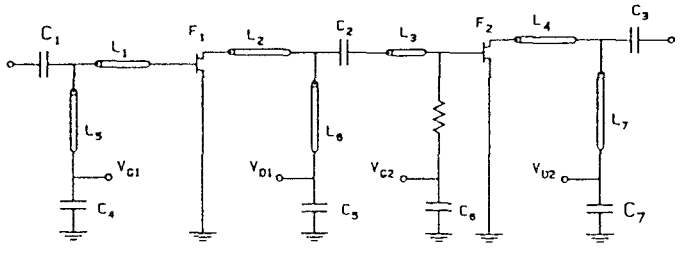

Fig. 8 - Equivalent circuit of the preamplifier

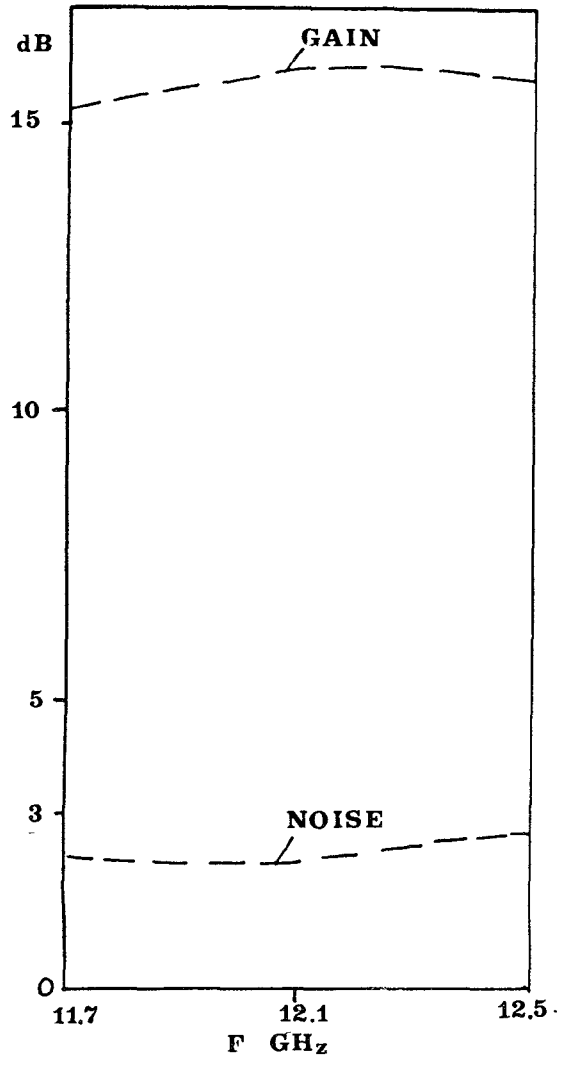

Fig. 9 - Performance of the monolithic preamplifier